Part 2 How it Works.

Overview.

The system comprises 4 element antenna and masthead preamplifier attached to a rotator on the vehicle roof. The antenna is coupled through the rotator to the reciever by a rotating transformer. Signals from the antenna are fed through a stepped rf attenuator which is graduated in 10dB steps from 0 to 100dB's and then to the receiver. As the antenna rotates, pulses from a shaft encoder produce a 256 steps/rev clock signal for the main control unit. A single pulse, once every rotation is also produced as a 'dead ahead' reset/syncronise marker. The motor in the rotator is controlled by sequence switches in the main control unit.
The receiver has two dedicated signal source outputs, one is a d.c.voltage directly proportional to received signal strength, the other being a direct audio output which is used to drive the noise detection system. The d.c. voltage is used to drive the deflection amplifiers on the crt display and to operate an 'S' meter on the unit's front panel. Neither of these outputs is affected by the position of the receivers volume control.

Fig.1 Main control unit and display

The main control unit contains a c.r.t. display which has a circular timebase divided into 256 radial positions. The rotation of the display is synchronised to the rotation of the antenna by the pulses from the shaft encoder. The instantaneous signal strength at each of these positions is stored in memory and used to deflect the crt beam, thus creating a frozen view of the signal strengths around the vehicle. Each new sweep of the antenna updates the memorised values, giving a succession of polar plots. The effect of this display is to show the direction of all signals arriving at the vehicle, their relative strength and quality.

Normally the system is used in *Signal* mode, utilising the varying d.c. voltage from the receiver to drive the display and the internal 'S' meter.
When the signals are very weak however, there is little or no deflection of the meter and so no d.c. to drive the display. The system can now be switched to *Noise* mode, this uses the full audio output from the radio, rectifying it to produce a d.c. signal that varies with the amount of quieting in the receiver. This d.c. voltage is then fed to the

display in the same way as in Signal mode. Using this mode the sensitivity of the system is extended by a further 20dB's.
The display has a single point (pip) marker, generated by adding a short pulse to the deflection signal . The marker's position can be manually rotated around the display using a front panel 'bearing' control, and is used to indicate the angle or 'bearing' (w.r.t. the vehicle) of the wanted signal.
The rotational position of this marker is transferred electronically to a handheld clear mapping device that contains 16 leds around it's periphery. An led is illuminated on the device, relaying the position of the bearing marker on the c.r.t.display.
The handheld device is held over the navigators map keeping the vehicle's position at its centre, and the direction of travel in line with the 'ahead' datum mark on the device. This way the direction of the incoming signal can be plotted onto the map. The hand held unit is equipped with map lamps for use in dark conditions.

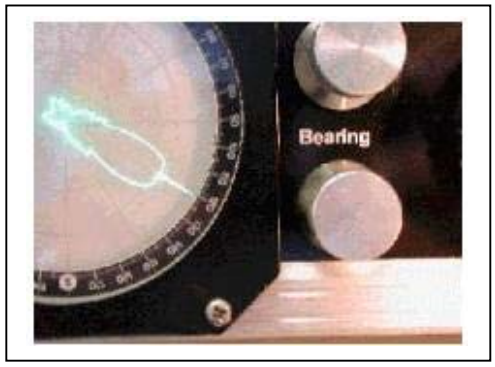


Fig 2. Display and corresponding map-wand readout .

Circuit description.

The circuit consists of several definable blocks:-
1) System clock and rotational position sensor.
2) The signal capture, digital storage and reconstruction circuitry.
3) Display timebase.
4) Handset driver circuitry

System clock.

The system clock is generated by a HP HEDS 5540 IO6, 512 Cycles/rev three channel optical encoder. This encoder is mounted at the bottom of the motor shaft that rotates the antenna. A small pcb mounted near the encoder divides the pulses by two producing 256 pulses per revolution to match the system's 8 bit architecture. The reset pulse is derived directly from the encoder's one pulse per revolution output. The encoder is oriented such that the reset/sync pulse is produced when the antenna is pointing 'dead ahead' of the vehicle, a mechanical worm adjustment is provided to calibrate the electronic/mechanical 'dead ahead' position. The output pulses from the encoder are positive going and are fed down a screened cable to the main unit that contains the pull up resistor pack for the encoder.

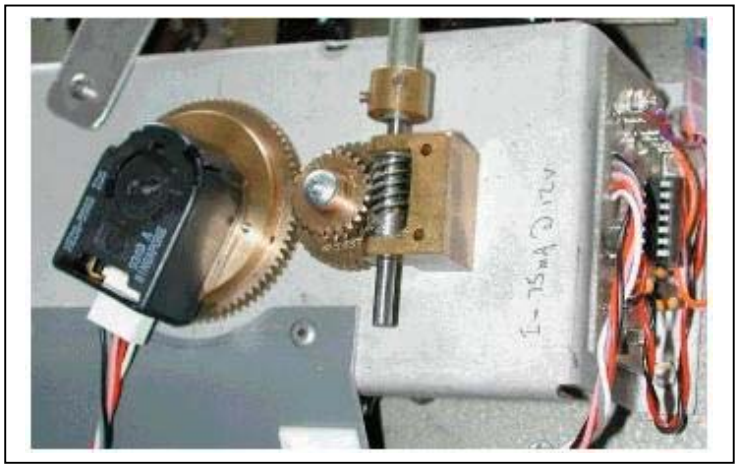
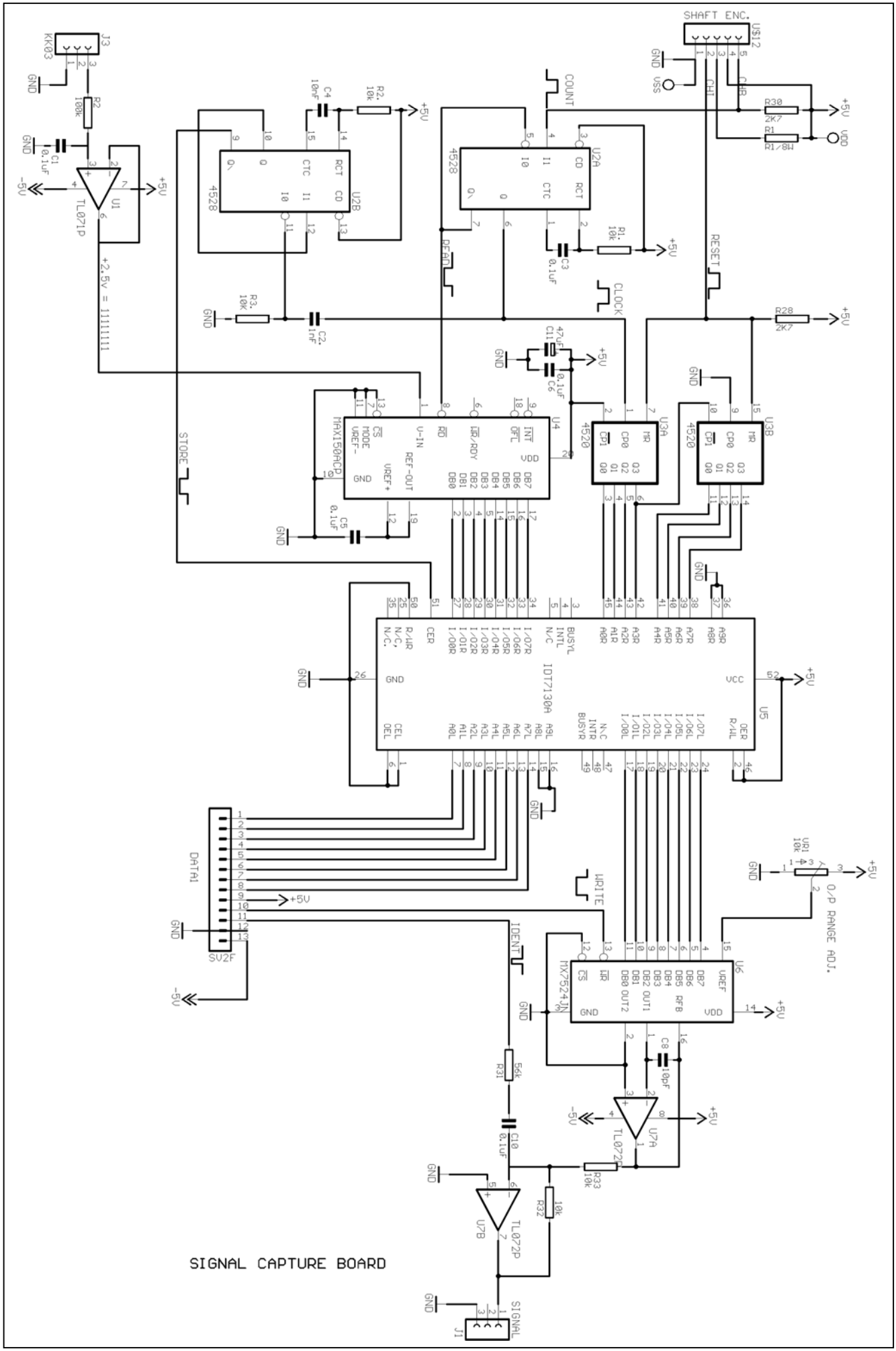


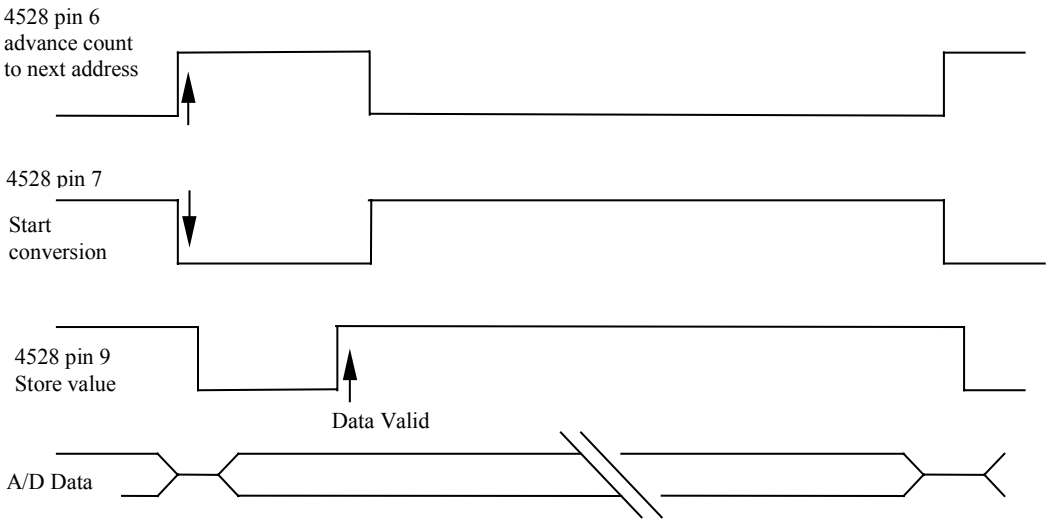
Fig.3 Shaft encoder and 'dead ahead adjustment

Signal capture and storage system.

The reciever that is used to monitor the 'off air' signals, has a signal strength circuit that has a wide dynamic range. This circuit produces a linear output voltage swing of Zero to 3.75 Volts over a 70dB r.f. signal strength variation.
This proportional d.c. voltage is fed, suitably scaled, into a buffer amplifier (U1) and then into the input of the A/D converter MAX150 (pin 1).


SHAFT ENC.
U$12
J3
KK03
R2
100k
C1
0.1uF
TL071P
U1
+2.5V = 11111111
C4
10nF
R2.
10k
4528
U2B
COUNT
U2A
R1.
10k
C3
0.1uF
DFAD
CLOCK
RESET
R3.
10k
C2.
1nF
R30
2K7
R1
R1/8W
R28
2K7
C11
47uF
C6
0.1uF
MAX150ACP
U4
4520
U3A
U3B
STOPE
C5
0.1uF
IDT7130A
U5
DATA1
SV2F
WRITE
IDENT
VR1
10k
O/P RANGE ADJ.
MX7524JN
U6
R31
56k
C10
0.1uF
C8
10pF
TL072P
U7A
U7B
R33
10k
R32
10k
SIGNAL
J1
SIGNAL CAPTURE BOARD

Pulses from the rotating optical encoder, arrive at the clock input (pin 4) of the 4528 dual monostable. (U2A) The monostable generates the following series of timing signals:-



When triggered by a step from the encoder, pin 6 of U2A increments the address counter U3 (4520) one count. This edge is also fed through network C2/R3 to the trigger pin of the second half of the 4528 to generate the $\overline{CE}$ (STORE) memory latch pulse on pin 9. As pin 6 goes high, pin 7 goes low, dropping the $\overline{RD}$ pin (8) of the A/D to start conversion. The instantaneous value of the signal strength is digitised by the converter. A short time later the data is valid, and as pin 9 (STORE) returns high this data is latched into the Dual Port RAM at that new address. As a continuous stream of encoder pulses flood in, the 8 bit counter stores 256 signal strength values in the DP RAM. The system continuously cycles round refreshing the memory with the latest signal value. To keep the rotational position of the antenna in sync with the rotating memory locations, a reset pulse from the encoder clears the address counter to zero,(4520 Master Reset) each time it reaches the 'dead ahead' position.

Reconstruction circuitry.

The Dual Port RAM as its name implies has two I/O ports and two address busses. Both the address busses point at the same memory locations allowing data to be written via one data bus at the same time as data is being read from a different location.
Bus arbitration logic is incorporated in the IC to intervene at the instance of an address clash.
This dual port system allows the data to be written into memory at the rotation rate of the antenna, whilst being read out at a much higher rate to generate a stable display, or artificial 'persistence' effect at the c.r.t. display.
The output data lines from the DP RAM are connected to U6, a MAX7524 D/A converter, which reconstructs a voltage proportional to the signal strength, this voltage is used to control the display deflection.
A 4520 counter (U10 A/B) on the display board, controls the output address lines of the DP RAM. The MAX7524's write pulse is also supplied by this second board.

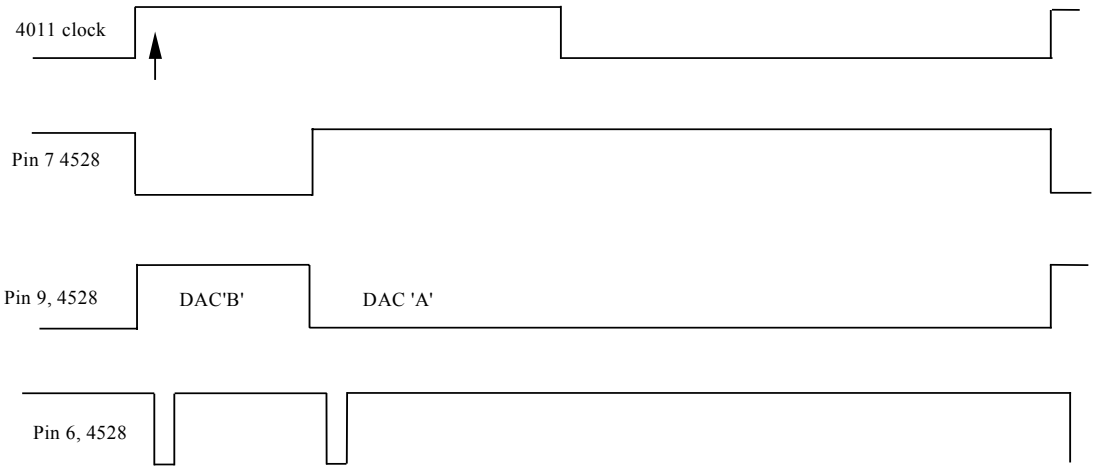
System Timebase.

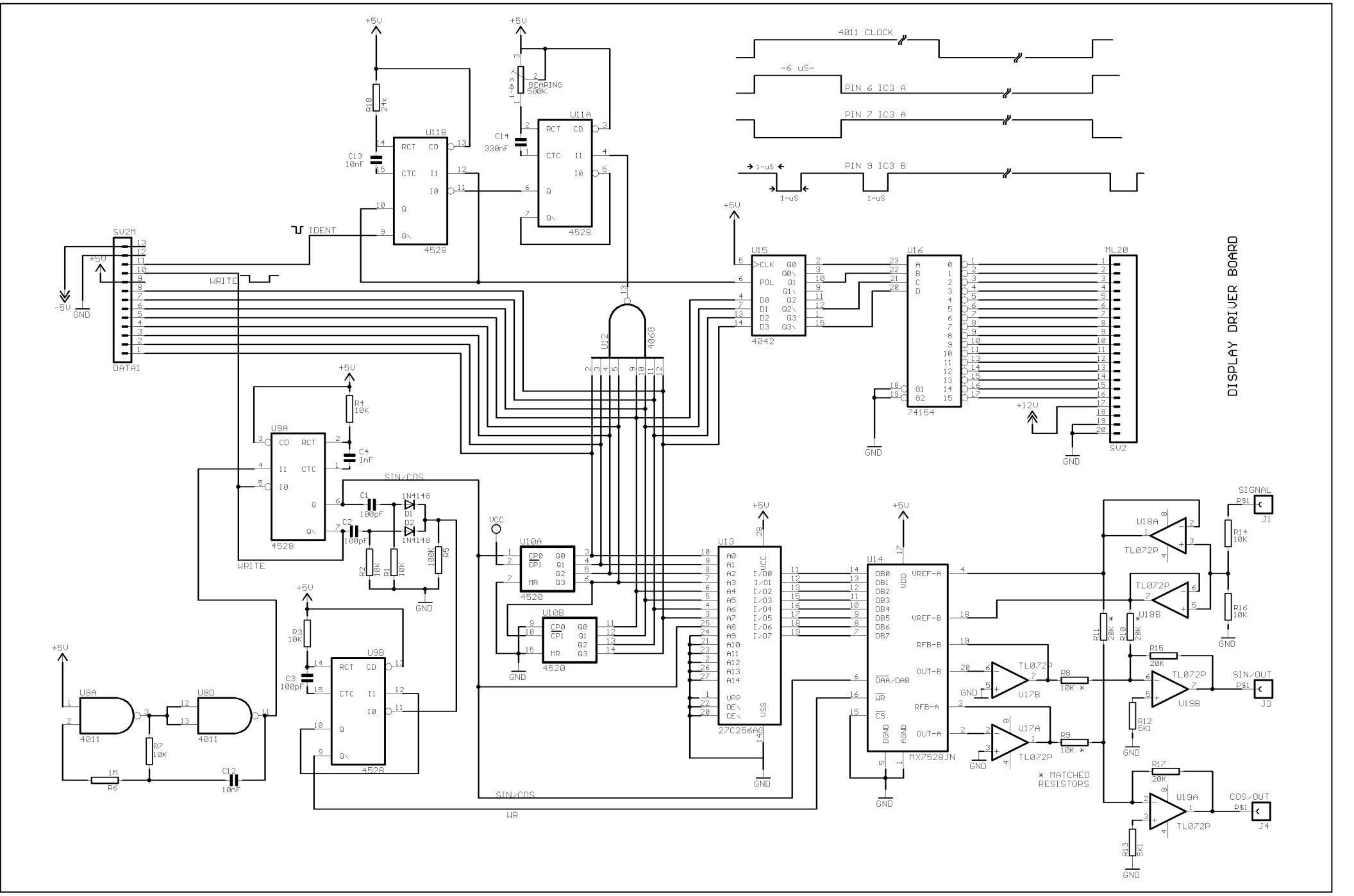
The timebase is generated by feeding a *sine* and *cosine* waveform to the X and Y deflection amplifiers of the c.r.t. display unit. By feeding the two waveforms to the c.r.t. in this way, a circlular timebase is generated on the screen.
The circuit is based on a dual multiplying D/A converter MAX7528 (U14), an EPROM 27C256 (U13) and an address counter 4520 (U10). The EPROM's architecture is arranged such that each address contains one 8 bit byte of data. The system uses the 8 least significant address lines of the EPROM to store a digitised *cosine* waveform with 256 points. The 9th address line (A8) when raised, allows A0 - A7 to access a second set of 256 memory locations which contain a digitised *sine* waveform of 256 points. Both waveforms are identical in amplitude.
Arranging the addressing in this way means that when A8 is high the *sine* data is able to be transferred to the D/A and when low, the *cosine*.
The EPROM input address lines are driven by the 4520 8 bit binary counter, and the output data lines from the EPROM are connected to the dual D/A converters' common input bus. The D/A converters A and B are controlled by the state of the single line $\overline{\text{DACA}}$/DACB, pin(6).

Reconstruction circiutry *continued*.

A free running clock constructed from two 4011 nand gates provide the trigger input for the 4528 (U9) timing generator. Both halves of this 4528 monostable are connected in non-retriggerable mode, with pins 7 connected to 5 and 10 to 12.
The first monostable when triggered by the rising clock edge (pin 4), creates the positive going CLK/SIN/$\overline{\text{COS}}$/ $\overline{\text{DACA}}$/DACB pulse at pin 6. The 100pF and 10k network creates a trigger pulse to the second half of the monostable through diode D1 to pin 11. As the first monostable times out, the network attached to the $\overline{\text{Q}}$ output pin (7), generates a second trigger pulse for U9B through D2.

The result being two 1uS $\overline{\text{W}}$/R pulses at pin 9, one just after the CLK/SIN/$\overline{\text{COS}}$/ $\overline{\text{DACA}}$/DACB line goes high, and one just after it goes low. (see timing diagram below




DISPLAY DRIVER BOARD
4011 CLOCK
-6 uS-
PIN 6 IC3 A
PIN 7 IC3 A
1-uS
PIN 9 IC3 B
IDENT
WRITE
SIN/COS
WR
BEARING 500K
* MATCHED RESISTORS
SIGNAL
SIN/OUT
COS/OUT
4528
4011
4042
74154
4520
4068
27C256AC
MX7528JN
TL072P
SV2M
DATA1
SV2
U8A
U8D
U9A
U9B
U10A
U10B
U11A
U11B
U12
U13
U14
U15
U16
U17A
U17B
U18A
U18B
U19A
U19B
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
C1
C2
C3
C4
C12
C13
C14
D1
D2
J1
J3
J4
+5V
-5V
+12V
GND
VCC

The operation of the circuit is as follows:-
4011 clock triggers the first monostable, this advances address counter 1 count, puts new *sine* data on the D/A bus from the EPROM and enables DACB. The second monostable generates a 1uS pulse that latches this data into DACB via its WR input (pin 16).
The first monostable now times out, dropping the CLK/SIN/$\overline{\text{COS}}$/ $\overline{\text{DACA}}$/DACB line, this changes to *cosine* data and enables DACA, a second 1uS $\overline{\text{W}}$/R pulse latches this data into DACA. Both converted waveforms appear at the D\A analogue outputs and pass to the X and Y amplifiers.
The output lines from the 4520 address counter are shared between the (sin/cos) EPROM and the DP RAM on the Signal Capture board. For the display to work correctly, the circular timebase has to be synchronised with the digitised signal strength values from around the vehicle. Using the same address counter for the display and the read address on the DP RAM ensures that the vector angle of the display is always locked to the correct place in memory.

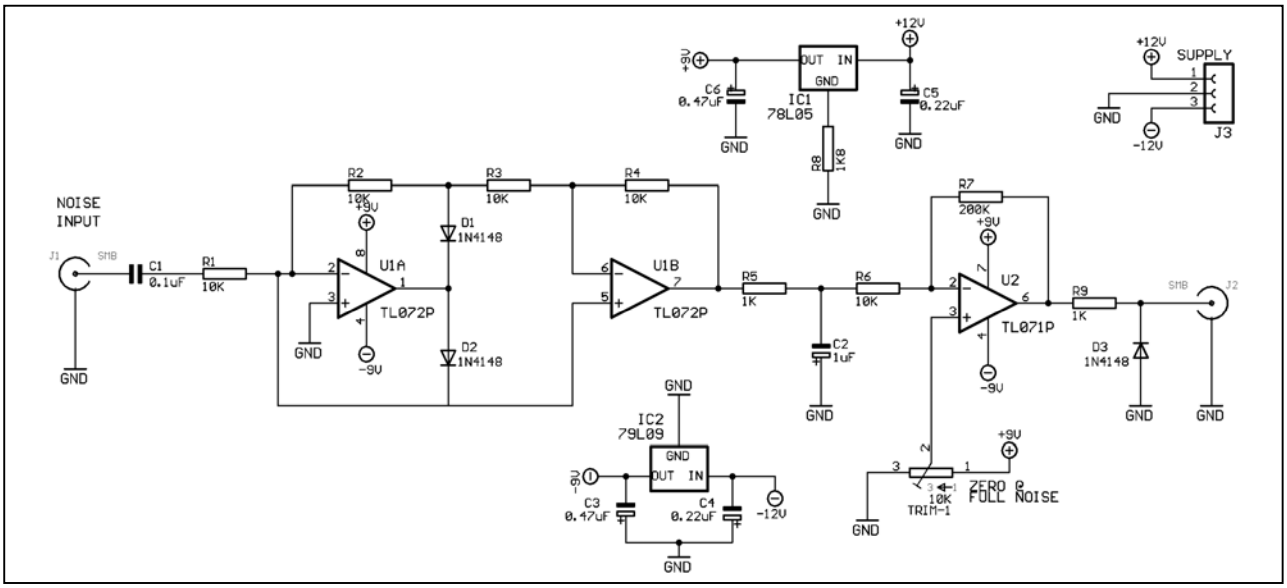
As the counter advances, pin (7) of the monostable U9A, generates a WRITE pulse which goes off to the Signal Capture Board to start conversion of the data for that particular position. The MAX7524 D/A output is taken through buffer amplifiers U7 and then to the multiplying inputs of the display dual D/As via the Signal input connector. So finally it can be seen that digitised signal strength values stored in memory are reconstructed and used to control the gain of the dual D/A converters. This has the effect of varying the amount of c.r.t. spot deflection in direct proportion to the signal strength whilst it is being rotated around the screen.

Handset driver circuitry.

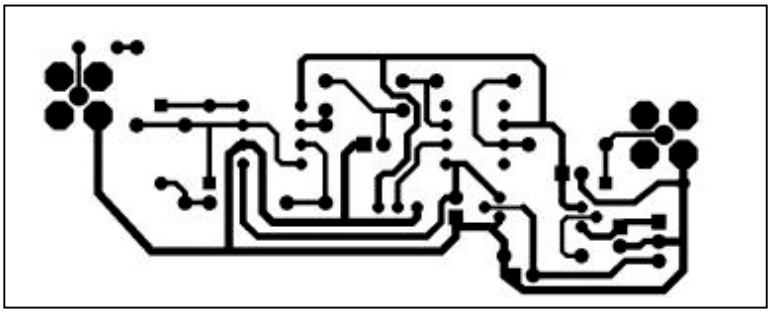
The 4520 address counter used to generate the display has its 8 output lines monitored by an eight input nand gate. This gate produces a high only when all the lines are at address zero. This condition produces the synchronisation pulse for the handset driver circuitry.
Dual monostable 4528 ‘B’, when triggered by the nand gate, is used to generate an *enable* pulse which can be delayed by the setting of the *Bearing* potentiometer. The 4 most significant lines of the counter are taken to 4042 latch which will capture the value of the counter output when the 4528 times out. The delay range is calculated such that counts from zero to 255 can be captured. The latched number is converted by a 1 from 16 line decoder driving the circular display of 16 led’s in the remote handset. As the bearing potentiometer is adjusted, a different led is illuminated in unison with the potentiometer’s position. A negative going version of the latch pulse is taken from pin (9) of 4528 ‘B’ and summed into to the buffer amplifier feeding the multiplying D/A’s control input. This pulse is added to the deflection voltage creating a marker ‘pip’ on the display, synchronised with the leds and the bearing potentiometer.

Noise detector circuit.

As mentioned in part one of this article, the dynamic range of the system was enhanced further by the addition of a noise detection circuit. Based on an 'absolute value' full wave rectifier, this circuit overcomes all the usual drawbacks of conventional 'discrete diode ' rectifiers. It has perfect linearity and responds to the smallest of input voltages making it ideal for detecting the slightest changes in quieting of the FM noise.



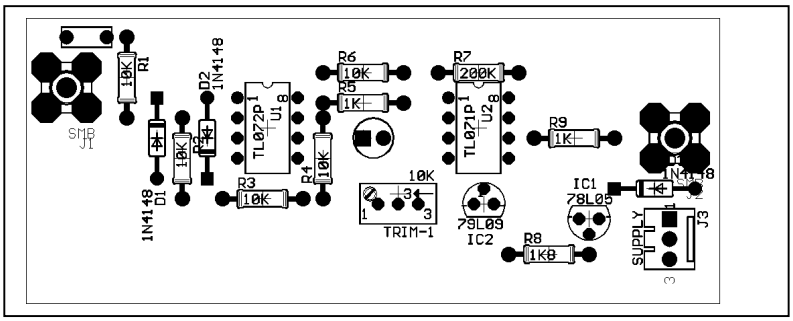
Equal value resistors are used throughout the circuit and additional input resistors could be added at the input to perform a summation of signals. Positive signals reverse bias D_2 and forward bias D_1 and the two inverting amplifiers are in cascade. Negative signals forward bias D_2 and reverse bias D_1 providing two feedback paths to U1A. The function of the circuit is described as $E_{out} = -E_{in}$.
The direct current output of the precision rectifier is fed to filter network R5/C2 to smooth the response for the deflection circuitry.



Noise detector board layout.

U2 is a x20 inverting amplifier which incorporates the introduction of an offset voltage. The offset trimmer is adjusted until the circuit gives 0V output for maximum un-squelched noise from the FM receiver. (No signal condition).

R_9 and D_3 are there to protect the deflection circuit from negative going levels.
The +/- 12 V system supply is regulated to +/- 9Volts by the two 100 mA regulators, removing any false response due to varying vehicle battery voltages.
Under test conditions the output of the circuit begins to rise from zero with only 0.5 db's of noise quieting.
The addition of this circuit has provided a 20 dB increase in the sensitivity of the system.



Noise detector component layout.

Conclusion.

Avoiding the use of microprocessors, this KISS approach to DF has proved extremely reliable and successful.
The entire system was developed over 2 seasons of DF hunting, with testing being carried out most Monday evenings and modifications incorporated in the intervening periods.
Using re-cycled parts wherever possible kept the cost to a minimum and made the whole project all that more enjoyable.
The most difficult part of the electronics construction was soldering the 52 pin PLCC Dual Port memory, although there is a DIP version available at the cost of greater board space.
Most of the other components are readily available from standard electronics suppliers or retail outlets. The operational amplifiers do not have any special parameters and can be substituted with ones that you have to hand.
The resistors R8 to 11 are easily matched using a cheap DVM.
The printed circuit boards were developed using Eagle layout editor from Cadsoft, from which, the schematics are copied in this document.
There were no complicated setting up procedures, the only adjustments needed were:-
Ensuring the 'S' meter dc voltage does not exceed the MAX150's input maximum of +2.5 volts by suitably attenuating the input.
The value of C14 on the 'Bearing' timer had to be 'adjusted on test', to get full 360° travel on the 'pip' marker.
And the O/P range trimmer should be adjusted on the MAX7524 to set the gain.